Design and prototyping of the readout electronics for the transition radiation detector in the High Energy Cosmic Radiation Detection facility*

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The High Energy Cosmic-Radiation Detection (HERD) facility is planned to launch in 2027 and scheduled to be installed on the China Space Station. It serves as a dark matter particle detector, a cosmic ray instrument, and an observatory for high-energy gamma rays. A transition radiation detector placed on one of its lateral sides serves dual purpose, (i) calibrating HERD's electromagnetic calorimeter in the TeV energy range, and (ii) serving as an independent detector for high-energy gamma rays. In this paper, the prototype readout electronics design of the transition radiation detector is demonstrated, which aims to accurately measure the charge of the anodes using the SAMPA application specific integrated circuit chip. The electronic performance of the prototype system is evaluated in terms of noise, linearity, and resolution. Through the presented design, each electronic channel can achieve a dynamic range of 0-100 fC, the RMS noise level not exceeding 0.15 fC, and the integral nonlinearity was less than 0.2%. To further verify the readout electronic performance, a joint test with the detector was carried out, and the results show that the prototype system can satisfy the requirements of the detector's scientific goals.

Keywords: HERD, dark matter particle detection, TRD, readout electronics, SAMPA, data acquisition, performance test

I. INTRODUCTION

Dark matter[1], cosmic rays[2], and high-energy gamma rays[3] are the particles of interest in physics and cosmology research. To detect the existence of dark matter and explore the origin of cosmic radiation, many experimental devices have been launched into space, including FERMI[4], AMS[5], CALET[6], CREAM[7], and JEM-EUSO[8]. China's first scientific experimental astrophysics satellite, the Dark Matter Particle Explorer (DAMPE), was launched on 17^{th} of December, 2015, marking the beginning of China's space-borne dark matter space exploration[9–15]. Although these devices have made outstanding scientific discoveries, there is still much exploration left to prove the existence of dark matter particles and gain deeper insights on the origin of the universe.

To improve the ability to detect dark matter and cosmic rays in space, the High Energy Cosmic-Radiation Detection (HERD) project has been proposed by scientists[16, 17]. HERD will be installed on the China Space Station in 2027, with the scientific goals of detecting dark matter, precision cosmic ray spectrum, and composition measurement[18]. Fig. 1(a) illustrates HERD's architecture, which consists of five detector systems: an electromagnetic calorimeter (CALO), the fiber tracker (FIT), a plastic scintillator detector (PSD), a silicon charge detector (SCD), and a transition radiation detector (TRD). The HERD is expected to operate on the space station for a decade[19]. The HERD can detect electron / photon with an energy range of 10 GeV - 100 TeV / 0.5 GeV - 100 TeV (e/γ); its primary cosmic ray nucleus detection range can reach 30 GeV – 3 PeV; its energy resolution can reach 1% at 200 GeV(e) and 20% at 100 GeV-PeV(p). These performance indicators are superior to those of contemporary space devices in operation[20–22]. For instance, HERD's instruments will extend the cosmic ray nuclear detection range by an order of magnitude and the nucleon energy resolution will be doubled compared to DAMPE; while compared to the FERMI satellite, HERD has higher sensitivity and a larger detection geometry factor. Thus, HERD is expected to produce essential research results during its operational lifetime.

The TRD is one of HERD's major subsystems and its primary scientific goal is to perform the absolute energy calibration of the CALO in the TeV energy range. The calibration operation will be carried out once in every 3-6 months, during which a mechanical turntable will rotate the TRD into the field of view of the CALO. The analysis of cosmic-ray proton events co-triggering the CALO and the TRD allows the transition radiation (TR) response of the TRD to be calibrated using the ground electron beam's TR calibration curve and consequently the CALO's absolute energy calibration. The calibration accuracy is expected to reach 10%. When the calibration is completed, the mechanical turntable will rotate the TRD out of the field of view of the CALO, and the TRD will be switched to the autonomous observation mode to perform gamma-burst observation and independent astronomical X-ray observations[23]. High-energy charged particles will enter the detector from the front and will be first converted into TR photons by the radiator, and then enter a gas detection

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cavity to realize the detection of TR photon signals. As shown in Fig. 1(b), the TRD consists of TRD detection units, readout electronics, a high voltage circuit, and its mechanical structure. The dimensions of the TRD are 650 mm (L) × 900 mm (W) × 250 mm (H), with a total weight less than 150 kg. The readout electronics of each unit are mounted on its side. The TRD detection unit consists of a regular radiator and a gas detector. Due to the limitation of the regular radiator area and the thickness of the drift region, the TRD cannot be designed as a single module. The complete TRD has six units arranged in a 3 rows and 2 column format. The signal from the detector will be read out via an anode, with a charge dynamic range of 100 fC. To guarantee the accuracy of detector measurements, the readout electronics system must exhibit an integral nonlinearity of less than 2% and maintain a noise level of less than 3 fC. Therefore, the electronics design is a challenge.

Conventional design of readout electronics generally uses either discrete components or application specific integrated circuit (ASIC) chips. However, there are strict constraints on board integration and power consumption in space-borne devices. Therefore, ASIC chips are more commonly adopted for these applications. Most of the commonly-used ASIC chips suitable for TRD dynamic range adopt designs such as APV25[24], PASA+TRAP[25], SPADIC[26], AGET[27], and SAMPA[28, 29]. After research, the SAMPA's ASIC chip was selected as the optimal choice for the TRD's readout electronics. Beacuse this chip's radiation resistance has been tested and it is proven to meet space operational requirements[30]. The SAMPA chip is a digital-analog hybrid ASIC with 32 channels and three dynamic ranges, namely 67 fC, 100 fC, and 500 fC. The power consumption of the CAS+ shaper of SAMPA is less than 8 mW, and the power consumption of its analog-to-digital converter (ADC) is 2 mW at 10 MSPS. In addition, a modular design with triple redundancy is adopted so that the chip can operate in space radiation environments.

A TRD detector prototype was developed with 64 readout channels. Therefore, two SAMPA chips will be needed for the TRD prototype's readout electronics. In this paper, the design and development of the prototype's readout electronics (PRE) for the TRD are discussed. In addition, the performance of the PRE was analyzed experimentally and a joint debugging experiment was carried out with the detector. The research results will discuss the suitability of the proposed PRE to HERD-TRD's designs.

II. HARDWARE DESIGN OF THE PRE

The PRE requirements for space applications differ from those of ground-based systems. Due to the complex operational environment, the space station's power consumption and hardware limitations, the front-end electronics require high speed, low power consumption, and high noise and radiation tolerance. Readout electronics for space-borne systems are expensive to produce, so it is necessary to design the prototypes first and validate

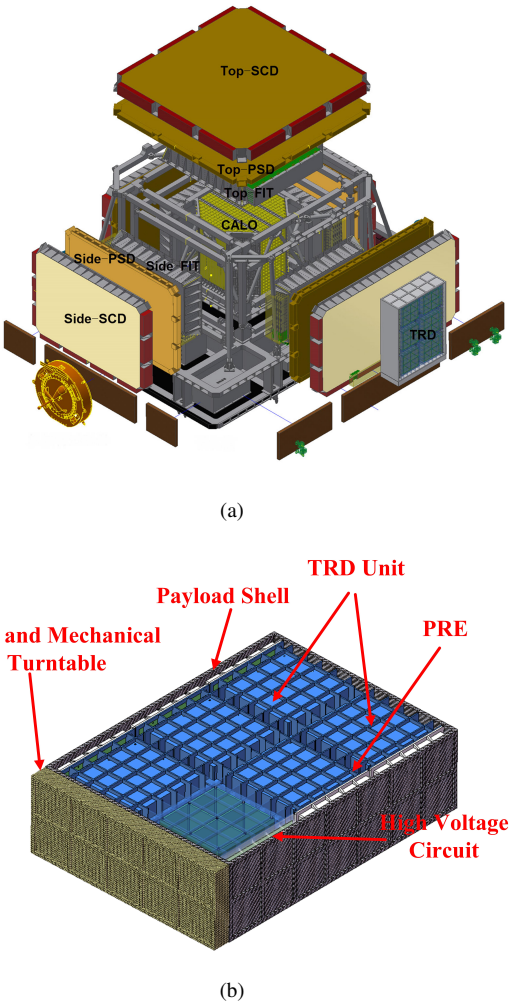
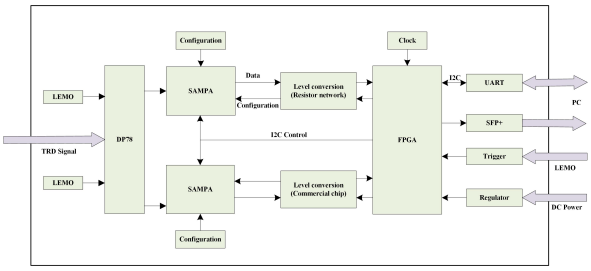


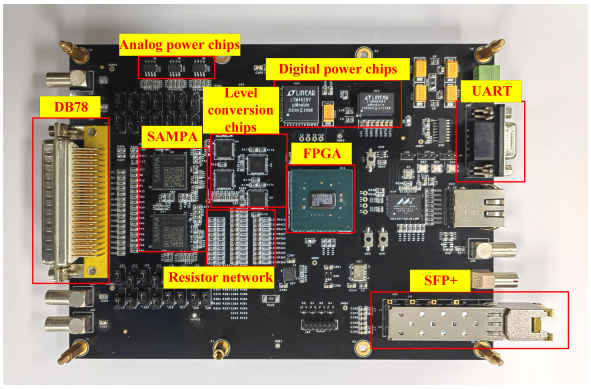
Fig. 1. (a) Structure of the HERD payloads. (b) TRD configuration.

the functionality of the design. The PRE uses the analog-digital mixed-mode ASIC chip, SAMPA to achieve low noise levels, highly reliable charge measurements, and digital-to-analog conversion. Moreover, the zero-suppression function integrated into SAMPA can realize data compression and decrease the transmission bandwidth. For the PRE, two SAMPA chips were used to realize 64 channels of detector signal readout. Fig. 2 shows the block diagram and photograph of the PRE, which includes the SAMPA circuit, a scalable low-voltage signaling (SLVS) and low-voltage differential signaling (LVDS) level conversion circuit, a field-programmable gate array (FPGA) circuit, the power management circuit, the communication interface circuit, and the detector signal interface circuit. The PRE uses a Xilinx Kintex7 XC7K70T-2FBG676I FPGA for control and data transmission[31]. The charge pulse signal generated by the detector is connected to the DB78 connector of the PRE through an interface board. The charge signal is integrated, shaped, and digitized at 10 MSPS in the SAMPA chip and the data are sent to the level conversion

circuit at a frequency of 320 MHz. The FPGA receives the data from the level conversion circuit, processes and packages it, and transmits it to a host computer through a Gigabit Ethernet link. In addition, the PRE can receive control commands and transmit parameter information to the host computer through a universal asynchronous receiver/transmitter (UART) interface. Through the UART interface, the PRE can be configured to operate in raw data or zero-suppression mode, and a series of tests were conducted in both modes to validate the system's operation.



(a)



(b)

Fig. 2. (a) Block diagram of the PRE. (b) Photograph of the PRE.

A. SAMPA ASIC

The SAMPA is a large-scale analog-digital hybrid ASIC designed by CERN for the upgraded front-end electronics system of the Time Projection Chamber (TPC) and Muon Chambers (MCH) in the ALICE experiment. SAMPA has good robustness to radiation and is suitable for radiated environments. A single SAMPA chip has 32 channels, and up to 11 data links can be selected for readout. The SAMPA structure is shown in Fig. 3 The chip is split into analog and digital signal processing subsystems, which are connected through an ADC.

The analog part mainly includes a positive / negative polarity charge-sensitive amplifier (CSA), a semi-Gaussian pulse shaper module, and a non-inverting stage. The feedback mechanism of the CSA consists of the capacitive feedback C_f and the resistive feedback R_f in parallel, and the amplified voltage signal is transmitted to the semi-Gaussian pulse shaper module for further processing. The shaper module includes a high-pass filter and two bridged-T second-order low-pass filters that produce a 4^{th}-order semi-Gaussian pulse. Internal registers are used to set the amplifier gain to 4 mV/fC, or 20 mV/fC, or 30 mV/fC. The shaping time settings available are 160 ns and 300 ns. Then, the shaper signal is digitized using a successive-approximation ADC, which can operate at sampling rates of 10 MHz or 20 MHz. The digital signal processor (DSP) section contains different digital filters, including three baseline correction modules, a tail cancelation module, and a data compression module. The DSP will package the data processed by the SAMPA chip and facilitate data extraction and verification through a 50-bit packet header[32]. SAMPA has 40 global registers and 30 channel registers (only accessible through the global register), which can be controlled through the inter-integrated circuit (I2C) bus protocol to configure the main functions of the chip or channels.

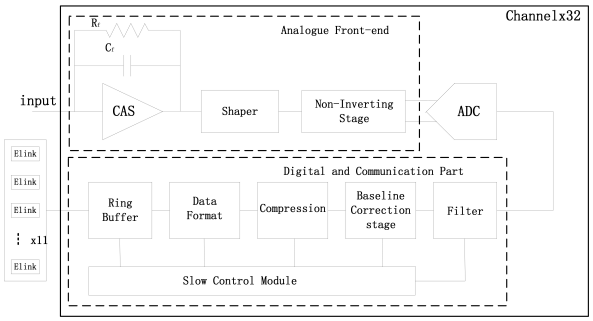


Fig. 3. Block diagram of the SAMPA chip.

B. Level Conversion Circuit

The serial communication link uniformly employs SLVS level conversion circuit, which includes 11 high speed differential data links, with clock and trigger links. SLVS is a special form of LVDS, with a lower common mode voltage (200 mV) and voltage swing (200 mV). The use of SLVS standard levels allows the SAMPA chip to reduce its power consumption. However, many FPGA chips do not support the SLVS standard, so SLVS and LVDS level conversion are required to communicate link data to the FPGA and provide SAMPA configuration information. For this purpose, two methods were adopted, namely an industrial conversion chip and a resistor network.

The commercially-available industrial chip method uses the MC20901 and MC20902 level conversion chips to achieve SLVS to LVDS matching and vice-versa. Both chips are high-performance bridge chips for FPGA that can achieve level matching of five signals on a single chip, supporting data rates up to 2.5 Gbps. On the other hand, resistor networks can achieve the same performance as that of the commercial chips. The resistance network is shown in Fig. 4, where Fig. 4(a) shows the conversion mechanism from SLVS to LVDS for communicating SAMPA data to the FPGA, while

the circuit Fig. 4(b) performs the opposite function. These networks are more resistant to radiation than commercial chips and have lower cost and power consumption. Therefore, resistor networks are adapted for future implementations instead of commercial chips.

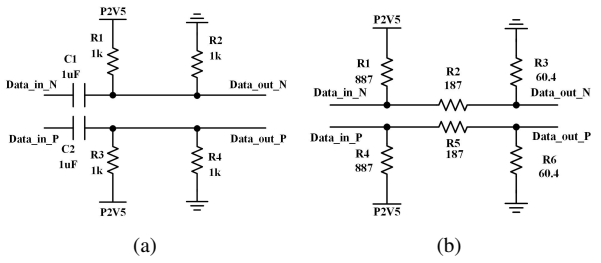


Fig. 4. Resistance networks for signal level conversion. (a) SLVS to LVDS level conversion. (b) LVDS to SLVS level conversion.

C. Interface Circuit

The TRD is a sealed gas detector and has strict sealing requirements. For the PRE implementation, a ceramic-encapsulated DB78 connector is adopted for signal transmission, and a PCB board-mounted connector is used on the PRE side. Aadditionally, to test the electronics performance, four standard LEMO connectors are used to lead out the four input signals of the SAMPA chip.

A highly reliable communication interface connection is required between the PRE and the host computer. The PRE's configuration commands downstream and status parameters upstream are transmitted through a UART interface operating in full-duplex mode. The scientific data transfer interface is designed to use a small form-factor pluggable (SFP) connector. The differential inputs and outputs of the SFP interface are directly connected to the FPGA's GTX. Connection to the host computer is via a 1000BASE-T SFP transceiver module and a Category 6 cable through the SiTCP network protocol processor. SiTCP is a hardware-based TCP processor for front-end readout electronics intended for applications where hardware space is limited[33], and can handle TCP, IP, and Ethernet protocols for data transmission.

D. Power Supply Circuit

To ensure the consistent operation of the PRE, a stable power supply is necessary. The board requires two power supplies, namely a 5 V and a 3.3 V supply, which are provided by an external power source. A set of power regulators provides the power required for the SAMPA, FPGA, and other onboard components. The lower supply voltages for the SAMPA are generated through low-noise linear regulators together with LC filter circuitry. Fig. 5 shows the power distribution architecture of the FPGA, SAMPA, and other chips. The Xilinx FPGA requires power for its power-on sequence. In the case of the PRE, power rails are designed to meet this requirement. The PGOOD pin of the DC-DC power supply is cascaded to the "Enable" pin of the subsequent power supply to complete the power-on sequence of the power supply. The power-on time is at most 50 ms according to the manufacturer, so a capacitor was added to the ground on the TRACK/SS pin to reduce the power-on time. The analog and digital circuits also contain two grounds, AGND and DGND, which are directly connected to the dedicated ground plane of the PCB. These designs ensure the stability of the PRE power supply.

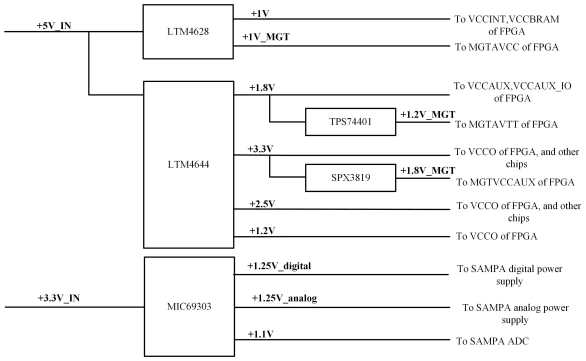


Fig. 5. Block diagram of the SAMPA power distribution circuit.

III. PRE FIRMWARE FUNCTION

The firmware functions of the PRE are implemented through its Xilinx Kintex-7 FPGA, which performs board control and data transmission. The two key functions of the PRE firmware are (i) to provide configuration and readout of internal registers, clocks and trigger signals for the two SAMPA chips, and (ii) to identify and package the detector-scientific data packets from SAMPA and pass them through the Gigabit Ethernet to the host computer. As shown in Fig. 6, the firmware function is divided into a command configuration unit, a data processing unit and a data transmission unit, which are analyzed further.

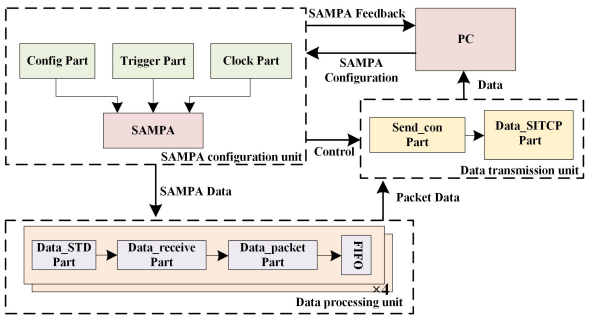


Fig. 6. Block diagram of FPGA logic design.

A. Command Configuration Unit

The SAMPA configuration unit is divided into three modules: the Clock Part, the Config Part, and the Trigger Part. The Clock Part is responsible for providing the system clock which is required for the entire firmware system operations and the SAMPA operating clock. SAMPA has a number of global and channel registers. Certain aspects of SAMPA's configuration and status can be controlled through these registers. The global registers can be directly controlled through the I2C interface, which is mainly responsible for configuring the key functions and status of SAMPA. Additionally, these registers can also set the configuration that is common to all channels. The channel registers available on each channel enable specific configurations of individual channels and can only be controlled through global registers. The Config Part transmits the configuration commands sent by the host computer to the IIC processing unit through the UART bus interface, packages them according to the protocol, sends them to the global registers inside SAMPA, and transmits the returned values to the host computer. SAMPA has two operating modes, namely an external triggering mode and an internal triggering mode. In the external triggering mode, the Trigger Part module will feed external trigger signals that meet the requirements into SAMPA, and the trigger signal will act as a data transmission control signal in the data transmission unit.

B. Data Processing Unit

SAMPA is a hybrid digital-analog chip with eleven digital signal serial transmission links capable of operating at 80 Mbps or 160 Mbps or 320 Mbps, which transmit the data stream to the data processing part. The data processing unit is responsible for acquiring the digital signal transmitted by SAMPA, analyze them to determine their header and tail portions. The unit determines the signal validity, package, process, and send the same to the data transmission module. In the design, the SAMPA operating clock is designed as a high-speed clock of 320 MHz, but it does not provide a data reference clock; therefore, high-speed signal acquisition at 320 Mbps is a challenge.

The data stream from the SAMPA to the FPGA uses double-edge sampling, and the phase between the data and the clock is calibrated through the internal IDDR and IODELAY parameters to avoid missing the setup and hold timings. To facilitate data alignment, the SAMPA chip generates synchronous signal packets with higher priority than data packets on each link under idle or mandatory commands. The sync signal is set by identifying the SAMPA internal sync packet, and the edge is replaced when the sync signal is pulled low. The edge changes only once because repeated changes do not solve the metastability problem. The synchronized data are passed to the subsequent Data_receive Part module. This module identifies the serial data, find the header and tail parts of the packet, filter out the synchronization packet and empty packets (if present). The data are converted into a 10-bit data transmission form for the Data_packet Part. The latter will then pack the 10-bit data into 64-bit packets and insert flag bits to identify their headers, tails and FIFO overflow parts to facilitate the subsequent data analysis. The final 64-bit data packets are transmitted to the following Data transmission module through the FIFO circuit.

C. Data Transmission Unit

The key functions of the data transmission unit are data summary and SiTCP transmission. These functions are mainly realized through two modules, Send_con Part and Data_SITCP Part. The data stream of all channels of SAMPA can be read from links 1-11 by configuring the internal registers. However, the peripheral circuits will become more complex as the transmission link increases, and the resultant power consumption of the circuit increases. Therefore, selecting the number of transmission links needs to consider the triggering rate, the transmission speed, and overall power consumption.

To achieve stable data reading in the external trigger mode at rates above 1 kHz and reduce the power consumption of the FPGA as much as possible, four links are used to read a chip, and each link carries eight data channels. The 320 Mbps high-speed data link aggregation was also an issue in the design. To solve this problem, a gatekeeper module was designed that generates a data transmission flag after the time window ends by delaying the trigger signal. This allows controlling the transfer window at a specific time and switching the transmission channel through the empty and full signals of the FIFO of each link in the Data processing unit. The FIFO's empty signal is monitored sequentially to ensure uninterrupted sequential readout. The readout data are aggregated into a deeper summary FIFO queue and then transmitted across clock domains to the SITCP transmission module, and finally to the host computer through the Gigabit Ethernet link.

IV. PERFORMANCE MEASUREMENTS

To explore whether the PRE design can meet the application requirements of the TRD, a series of tests was performed using the PRE's raw data and zero-suppression modes. These included a baseline characterization test, a channel linearity test, an amplitude resolution test, a crosstalk test, a long-term operational stability test, an equivalent noise level test under different input signals, and a joint detector test. The test results were analyzed to evaluate the performance of PRE and verify the reliability of the design. For the tests, the SAMPA was configured to operate at 320 MHz clock rate, the ADC sampling clock was set to 10 MHz, the internal charge-sensitive preamplifier gain was set to 20 mV/fC, the shaping time was set to 160 ns, and the negative charge is collected. The test input pulse signal and trigger were generated using a signal generator (Tektronix AFG31000). The pulse signal output simulated

the charge signal generated by the detector pad. During the test, voltage-to-charge conversion was realized using a charge converter board. A bank of sixty-four capacitors of 1 pF each is placed on the charge converter board to convert the voltage pulses from the signal source to charge signals, which were then input to the analog pins of the SAMPA through the DB78 connector for testing. The input test signal was set up as a negative polarity pulse signal with a rising edge of 30 μs, a falling edge of 2 ns, a pulse width of 50 μs, and a voltage range of 0-100 mV; this resulted in a charge $(Q = C \times V)$ being injected through the capacitor to generate a charge signal of 0-100 fC. The trigger signal was a square wave with an amplitude of 3.3 V and a pulse width of 200 μs. The input pulse signal is delayed by 10 μs from the trigger signal to prevent incomplete signal acquisition.

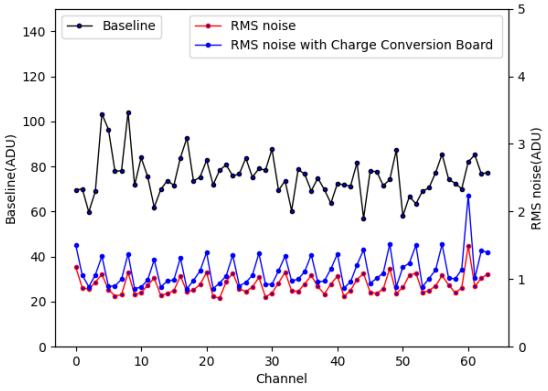


Fig. 7. Baseline and RMS noise levels of the PRE.

A. Baseline Noise Characterization

Noise characterization refers to the modeling of the random perturbations introduced during the signal transmission and processing, and is of great significance for interpreting experimental results, electronic model verification, and physical information extraction. Baseline noise testing is used to quantify system noise levels and evaluate the reliability of electronic data. To avoid the undershoot phenomenon at the trailing edge of the pulse signal, which could affect the regular operation of the SAMPA's DSP module, the input signal of SAMPA was superimposed on the baseline level in the analog front end.

During the test, a baseline noise analysis of the 64 channels of the two SAMPA chips of the PRE was carried out. The acquisition time window was 10 μs, with a trigger frequency of 1 kHz. This was aimed to simulate the state of the TRD detector when it is in orbit during the calibration of the electromagnetic Calorimeter and the transmission of uncompressed raw data. The level of noise was characterized through its Root Mean Square (RMS) value.

Fig. 7 illustrates the baseline data and corresponding RMS noise levels. The black line represents the baseline levels, which were in the range of 60-110 ADC codes. The red line represents the RMS noise of the electronics, and the blue line represents the change in RMS noise with the addition of the charge conversion board. The acquisition time for each test was one minute. From Fig. 7, it can be seen that connecting the charge conversion board to the PRE will introduce some noise. The RMS noise of the PRE is below 1.5 ADC code (which is equivalent to 0.15 fC), and is increased to less than 2.5 ADC code (equivalent to 0.24 fC) after the board is connected. Due to the limited space for installing electronics in the space station, the charge conversion board or cable will be connected between the PRE and the detector to achieve a more compact configuration. This indicates that the future adapter board or cable designs should focus on reducing the noise introduced.

B. Channel Linearity Test

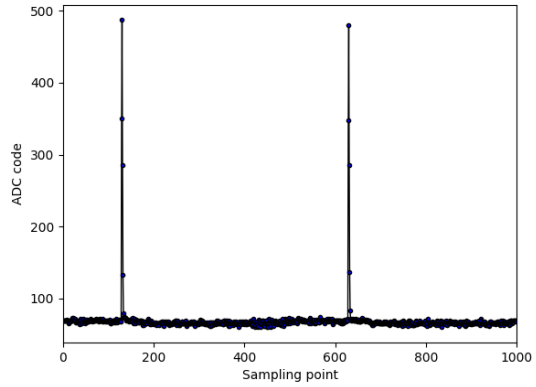
Ideally, the relationship between the input and output of a readout electronics system is a linear function of positive proportion, whose slope represents the magnification of the readout system. Integral nonlinearity refers to the nonlinear distortion introduced by the channel during the integration of the input signal, and this distortion can be used to evaluate the linearity of a readout electronics system.

A voltage pulse was generated using the pulse signal generator and sent to the charge conversion board to generate charges of 0-100 fC in steps of 10 fC. The PRE was set to operate in zero-suppression mode with the threshold set to 10 ADC codes beyond the baseline, at a trigger frequency of 1 kHz and a sampling time window of 100 μs. Due to the limited transmission bandwidth available at the space station, waveform accumulation, compression and peak finding may be required on the waveform obtained by each channel. After accumulation, the waveform's linear expression is fitted to calculate the integral nonlinearity. Fig. 8(a) shows the waveform of the acquired input at 50 fC, while Fig. 8(b) shows a randomly-selected channel, whose integral nonlinearity was 0.16%.

C. Amplitude Resolution Test

Amplitude resolution indicates the electronics system's ability to resolve different input signal amplitudes and equivalently characterizes the energy resolution for the system. The TRD will use the linear relationship between the cross-radiation response of charged particles and the Lorentz factor to perform absolute energy calibration of the electromagnetic calorimeter in orbit, so it requires the readout system with high-precision energy resolution.

For this test, the input charge was set in the range of 0-100 fC in steps of 10 fC. Waveform fitting was performed using the 4^{th} order semi-Gaussian pulse to obtain the amplitude



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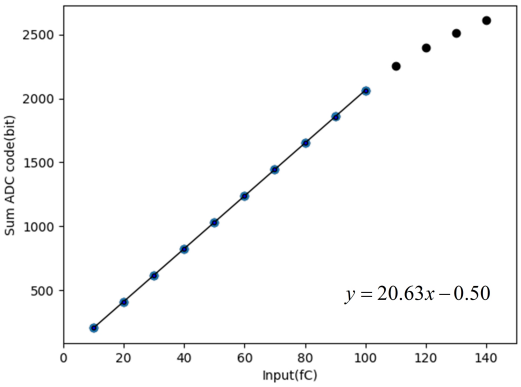

(b)

Fig. 8. (a) Output waveform for a 50 fC input signal and (b) linearity test results of the PRE.

resolution curve of the PRE as[34],

$$f(x) = a(\frac{x-t}{\tau})e^{-N(\frac{x-t}{\tau})} + Bl \quad (1)$$

where N is the shaping order, which is set to 4, τ is the peak time, Bl is the baseline, t is the start time and Ae^{-4} is the amplitude.

Fig. 9 shows the amplitude resolution of the PRE at different input amplitudes where the resolution of the system after 10 fC is better than 3%.

D. Equivalent Noise Level Test under Different Input Signals

A 2-10 fC charge signal was generated using the signal source at a step of 2 fC and a 20-100 fC signal at a step of 10 fC. A scan test was conducted to observe the equivalent noise level (ENL) change under different input charges. The frequency of the input signal was set to 1 kHz. The SAMPA gain was set to 20 mV/fC in the test, and each charge value was tested in zero-suppression mode for one minute. The RMS value represents the ENL of the PRE. Fig. 10 shows

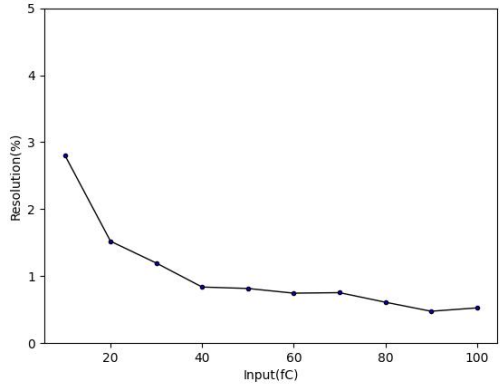

Fig. 9. Amplitude resolution of the PRE.

the ENL curve of a PRE channel. The amount of input charge is presented on x-axis, while the y-axis shows the RMS percentage compared to the measured mean value. It can be observed from the figure that the relative noise level tends to decrease as the input signal increases.

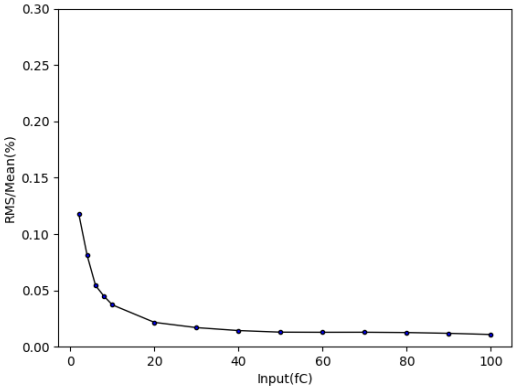

Fig. 10. The ENL test under different input charge.

E. Crosstalk Test

The channel-to-channel crosstalk in a readout electronics system represents the interference effect of a channel on the signal to its adjacent channels. Crosstalk will introduce additional noise during signal transmission and measurement, thus affecting the signal quality and possibly causing distortion and measurement errors. During the test, a single SAMPA channel was injected with a charge, while the remaining channels were left floating. The input pulse signal is 100 mV, and its equivalent input charge is 100 fC, the maximum input range at a gain of 20 mV/fC of the SAMPA. After calculation, the crosstalk coefficients of the adjacent channels were 0.023% and 0.011%, which show that the impact of crosstalk was negligible.

F. Data Reading Stability Test

A data reading stability test system was set up to demonstrate the reliability of data transmission and interconnection using the PRE, a signal source and a host computer. The frequency of the signal source was set to 1 kHz. To perform this test, the system was operated in zero-suppression mode for one week, and a linearity test was performed every day at 9 a.m. and 9 p.m. In the offline data analysis, the test data were linearly fitted using a first-order linear fit coefficient to determine the stability of the gain. Fig. 11 shows the coefficients of the linear fit over time for one SAMPA channel, and it can be seen that the gain is relatively stable. The entire system operated stably without any data packet loss.

G. Joint Test with TRD

To verify the performance of the PRE design, conducting a joint test with the TRD was necessary. Internally, the working gas of the TRD was $97\%Ar + 3\%C_4H_{10}$. The experimental platform was built as shown in Fig. 12. The test system included the PRE, a TRD, a high-voltage power supply, a low-noise digital power supply and a host computer. During the test, cosmic rays were used to test and verify the system at first. Then, a ^{55}Fe radioactive source was used for testing. In the cosmic ray test, the external trigger signal for the electronic system is generated using a plastic scintillation detector (PSD) which is then fed to the PRE. Fig. 13(a) shows the cosmic ray energy spectrum of the TRD, which conforms to the Landau distribution. Fig. 13(b) shows the ^{55}Fe energy spectrum when a high voltage of 6200 V was applied to the detector cathode and a high voltage of 1800 V was applied to the thick gaseous electron multiplier (THGEM). For this test, the SAMPA chip is configured in the self-triggered mode with a sampling time window of 100 μs. The gain of the SAMPA chip was 20 mV/fC. The measured energy resolution of signal integral is 29.3% for full-energy peak (5.9 keV energy). The peak of the cosmic ray is approximately one-third of the ^{55}Fe full-energy peak. The test demonstrates the feasibility of applying the SAMPA chip to TRD, and the designed TRD prototype readout electronics system achieved its intended purpose.

V. CONCLUSION

In this paper, a PRE design suitable as the TRD detector for the HERD project of the China Space Station is proposed and validated. This PRE has 64 channels and a total power consumption of 6.26 W. The PRE mainly consists of a detector interface circuit, a SAMPA chip and its peripheral circuits, SLVS and LVDS level conversion circuits, an FPGA circuit, a power management circuit, and a communication interface circuit. The tests performed indicate that the PRE system performed well. The baseline noise level of the 64 channels is low, with the RMS noise level being less than 1.5 ADC code, which accounts to only 0.15% of the dynamic range of the PRE. The integral nonlinearity of the channel was less than 0.2%, and moreover, the amplitude resolution also meets the design requirements. To further verify the performance of the PRE, it is coupled to the TRD. The results from the cosmic ray test serve as evidence that the PRE is functioning effectively. Energy resolution of 29.3% is obtained with a ^{55}Fe radioactive source for 5.9 keV energy. According to this, the PRE design can meet the needs of TRD readout and can constitute a basis for future engineering design of relevant systems.

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Author Contributions All authors contributed to the study conception and design. Material preparation, data collection, and analysis were performed by Jie-Yu Zhu, Yang-Zhou Su, Hai-Bo Yang, Fen-Hua Lu, Yan Yang, Xi-Wen Liu, Ping Wei, Shu-Cai Wan, Hao-Qing Xie, Xian-Qin Li, Hui-Jun Hu, Hong-Bang Liu, Shu-Wen Tang and Cheng-Xin Zhao. The first draft of the manuscript was written by Hai-Bo Yang, and all authors commented on versions of the manuscript. All authors have read and approved the final manuscript.

Data Availability Statement The data that support the findings of this study are openly available in Science Data Bank at https://cstr.cn/31253.11.sciencedb.j00186.00474 and https://www.doi.org/10.57760/sciencedb.j00186.00474.

Conflict of interest Cheng-Xin Zhao is an editorial board member for Nuclear Science and Techniques and was not involved in the editorial review, or the decision to publish this article. All authors declare that there are no competing interests.

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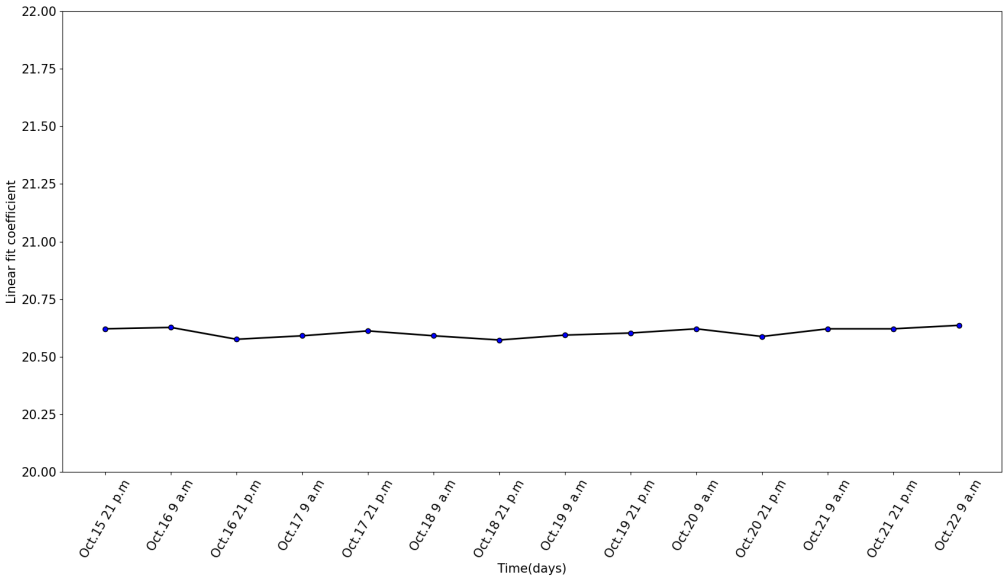

Fig. 11. Stability test of the PRE channel over long-term operation.

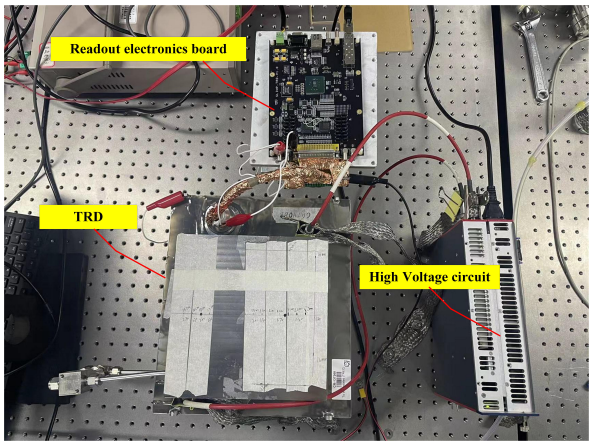

Fig. 12. Experimental platform of joint test with TRD.

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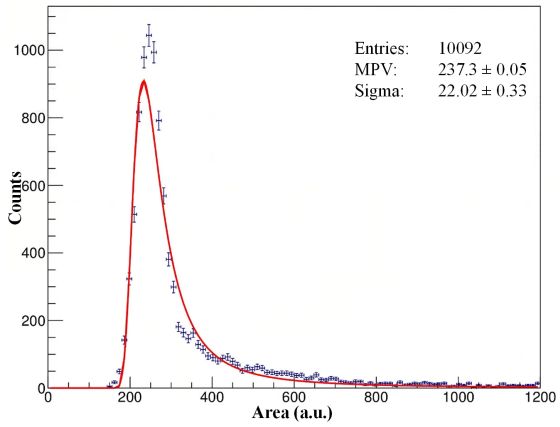

(a)

(b)

Fig. 13. (a) Energy spectrum with cosmic ray. (b) Energy spectrum with ^{55}Fe radioactive source.

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